UNIVERSITY OF SASKATCHEWAN

Department of Computer Science

CMPT 215.3 FINAL EXAMINATION

December 19th, 2000

Total Marks: 100

CLOSED BOOK and CLOSED NOTES
NO CALCULATOR

Time: 3 hours

Instructions

Read each question carefully and write your answer legibly on the examination paper. **No other paper will be accepted.** You may use the backs of pages for rough work but all final answers must be in the spaces provided. The marks for each question are as indicated. Allocate your time accordingly.

Ensure that your name AND student number are clearly written on the examination paper and that your name is on every page.

Note: a reference table of MIPS instructions is provided at the end of the examination paper.

Question	Marks
1 (10 marks)	10
2 (16 marks)	16
3 (16 marks)	16
4 (20 marks)	20
5 (20 marks)	20
6 (18 marks)	17
Total	

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1. **General** (*10 marks in total – 1 mark for each part*) Give the technical term that best fits each of the following descriptions or definitions.

   (a) An operation that tells the assembler how to translate a program but does not produce machine language instructions; always begins with a period.

   Assembler directives

   (b) The field in the IEEE 754 standard for floating point number representation that stores the digits of the fractional part.

   Significand

   (c) A cache replacement scheme in which the item replaced is the one that has been unused for the longest time.

   LRU

   (d) A technique that uses main memory as a "cache" for programs stored on disk.

   Virtual memory

   (e) An event that unexpectedly changes the normal flow of instruction execution; as, for example, when a program tries to perform an invalid operation (such as a "lw" to a non-word address), and the operating system must be invoked.

   Exception

   (f) An advanced pipelining technique that enables the processor to fetch and execute more than one instruction per clock cycle.

   Superscalar

   (g) A type of digital logic circuit without "memory"; the output is a function *only* of the current input.

   Combinational

   (h) In an assembly language program, a label referring to an object that can be referenced from files other than the one in which it is defined.

   External (labeling)

   (i) A technique for dealing with data hazards, wherein a result value from a preceding instruction is provided directly to the instruction that needs it, rather than waiting for the result to be written to memory or to the register file.

   Forwarding

   (j) A field in each entry in a processor cache that contains the address information required to determine whether the block stored there is the one being searched for.

   Tag

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2. **Computer Performance** (*16 marks in total*)

   (a) (*2 marks*) List two different types of benchmarks.

   Kernel and synthetic
   (Real applications)

   (b) (*2 marks*) For a particular program as run on a particular system, the number of machine language instructions executed is 200 x 10^8, the clock rate is 500 MHz, and the CPU execution time is 80 seconds. What is the CPI?

   $CPU = \frac{(\# instr)\ CPI}{clock\ rate}$ $CPI = \frac{CPU \cdot clock\ rate}{\#\ of\ instr}$

   $CPI = \frac{80 \cdot 500 \times 10^6}{200 \times 10^8} = \frac{40}{20} = 2$

   (c) (*6 marks*) For each of the following parts, suppose that you have obtained some measurements of the performance of a system before and after a system change was made. Your task is to determine what type of change was made, among the following possibilities: coding changes to the high level language program being tested, **or** new processor with the same instruction set architecture, **or** new processor with a different instruction set architecture. In each part you are to assume that only one of these types of change has been made, so you **must** indicate only **one** of these changes for each part to get any credit.

   $CPU_{old} = \frac{c}{Mips}$ $CPU_{new} = \frac{c}{x\ Mips} = \frac{1}{x} CPU_{old}$

   (i) Suppose that the MIPS value for the measured program has increased by 50% and the CPU execution time has decreased by 33%. What is the most likely type of system change that was made, from the possibilities given in the above list?

   $CPU_{new} = \frac{c}{1.5\ MIPS} = \frac{2}{3}$ $\frac{c}{MIPS} = \frac{2}{3}$ new processor w/ same ISA

   (ii) Suppose instead that the MIPS value for the measured program has increased by 25%, the CPU execution time has decreased by 5%, and the CPI has decreased by 20%. What is now the most likely type of system change that was made, from the possibilities given in the above list?

   Coding changing to program

   (iii) Suppose instead that the MIPS value for the measured program has increased by 25%, the CPU execution time has decreased by 20%, and the CPI has decreased by 10%. What is now the most likely type of system change that was made, from the possibilities given in the above list?

   new processor w/ different ISA

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(d) (*2 marks*) Would you expect a CISC or a RISC processor to have a higher MIPS rating, assuming similar age (year of design), design effort, and cost?

RISC - Reduced Instruction Set Computer

(e) (*2 marks*) Suppose that the following CPIs and frequencies of usages have been determined for the four instruction classes of a particular processor. By what percentage would the MIPS rating increase if a hardware improvement was implemented that decreased the CPI for instructions of class D from 5 to 2 (without changing anything else)?

Instruction class	CPI	Frequency
A	4	10%
B	1	50%
C	3	20%
D	5	20%

$CPI_{old} = .4 + .5 + .6 + 1.0 = 2.5$

$CPI_{new} = .4 + .5 + .6 + 0.4 = 1.9$

$MIPS = \frac{Clock Rate}{CPI \; 10^6} = \frac{c}{CPI}$

$\frac{MIPS_{new} - MIPS_{old}}{MIPS_{old}} = \frac{\frac{c}{CPI_{new}} \; \frac{c}{CPI_{old}}}{\frac{c}{CPI_{old}}} = \frac{\frac{1}{CPI_{new}} - \frac{1}{CPI_{old}}}{\frac{1}{CPI_{old}}} = \frac{CPI_{old}}{CPI_{new}} - 1 = \frac{2.5}{1.9} - 1 = \frac{6}{19} = 32\%$

(f) (*2 marks*) Consider a particular program that spends 20% of its execution time on floating point instructions. Write an expression for the percentage by which total execution time would be decreased, if the time it takes to execute each floating point instruction was decreased by p %.

$T_{old} = T_0$

$T_{new} = .8 T_0 + .2\left(1 - \frac{p}{100}\right) T_0 = T_0 - \frac{0.2p}{100} T_0 = \left(1 - \frac{0.2p}{100}\right) T_0$

$\frac{T_{new} - T_{old}}{T_{old}} = \frac{\left(1 - \frac{0.2p}{100}\right) T_0 - T_0}{T_0} = - \frac{0.2p}{100} \quad \therefore \frac{p}{100} \times 20\%$

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3. **Arithmetic** (*16 marks in total*)

(a) (*3 marks*) In IEEE 754 floating point format, what are the special meanings of exponent field values of 00…0 and 11…1?

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00…0 - denormalized # (when significand ≠ 0)
0 if significand = 0
11…1 - NaN (significand ≠ 0)
infinity (significand = 0)

(b) (*3 marks*) Give a truth table for a logic function whose 3 inputs are the binary digits of a 3 bit signed integer *x* and whose 3 outputs give the binary digits of –*x*. Assume signed integers are represented using 2's complement, and ignore overflow.

x_1	x_2	x_3	y_1	y_2	y_3
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	0	0	1

```
  001
  110
+   1
-----
  111
```

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(c) (*8 marks*) Give the base 10 number that is represented by 110010, assuming each of the following representations: Look at my midterm

(i) 6 bit 2's complement

-14

(ii) 6 bit biased notation with bias of 31

19

(iii) 6 bit 1's complement

-13

(iv) 6 bit sign-magnitude

-18

(d) (*2 marks*) Recall that in the IEEE 754 floating point standard, single precision floating point numbers have a 1 bit sign field, followed by an 8 bit exponent field (in biased notation with a bias of 127), followed by a 23 bit field giving the digits of the fractional part. What decimal number is represented by 11000000110110000000000000000000?

$$(-1)^1 \cdot \underbrace{1.1011_2}_{1.6875} \cdot \underbrace{2^{(129-127)}}_{4}$$

$$(-1) \cdot 110.11_2$$

$$-6.75$$

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4. **Machine and Assembly Language** (*20 marks in total*)

(a) (*2 marks*) Describe what is done within each pass of a 2 pass assembler.

ps. A12

(b) (*2 marks*) Suppose MIPS had 64 general-purpose registers rather than just 32. What impact would this have on the design of MIPS machine language?

Would have to use 6 bits in rs, rt, rd in R and I formats and use less for shamt and displacement.

(c) (*4 marks*) Write a well-structured fragment of C or Java or Eiffel code that accomplishes the same task as the following sequence of MIPS assembly language instructions. Use the variable "i" for register \$s1, "n" for register \$s2, and an integer array "A" (indexed from 0 to n-1) for the sequence of words whose starting memory address is initially in \$s3. Your code should result in the same final assignment to "i", as is made to register \$s1.

```
      add    $s1,$s2,$zero
L:    beq    $s1,$zero,out
      lw     $t1,0($s3)
      beq    $t1,$zero,out
      addiu  $s3,$s3,4
      addi   $s1,$s1,-1
      j      L
out:  add    $s1,$s1,$s1
```

for (i=n; i!=0 && A[n-i]!=0; i--);
i+=i;

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(d) (*12 marks*) Write a MIPS procedure that "reverses" an array. Specifically, your procedure should take two parameters. The first parameter (passed in $a0) is the starting memory address of an array of words. The second parameter (passed in $a1) is the number of items in the array. Your procedure should reverse the array by exchanging its first and last items, then the second and second last items, and so on. For example, if your procedure is passed the address of the array 1 8 3 5 3 0, with the number of items being 6 in this case, your procedure should transform this array into 0 3 5 3 8 1.

```
      addi   $a1, $a1, -1
      add    $t1, $a1, $a1
      add    $t1, $t1, $t1
      add    $t0, $t1, $a0
loop: lw     $t1, 0($a0)
      lw     $t2, 0($t0)
      sw     $t2, 0($a0)
      sw     $t1, 0($t0)
      addi   $a0, $a0, 4
      add    $t0, $t0, -4
      j      loop
done: jr     $ra
```

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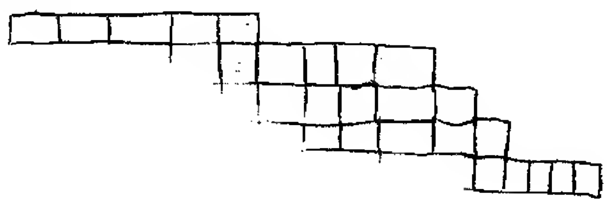
5. **Datapath and Control** (*20 marks in total*)

(a) (*4 marks*) Determine the **total** number of clock cycles required to execute the program segment given below using a 5-stage pipeline **without** forwarding. The five stages and their functions are given as follows:

- IF - instruction fetch (from instruction memory)
- ID - instruction decode and register file read
- EX - execute or address calculation
- MEM - memory access (from/to data memory)
- WB - write back to register file

Assume that if one instruction reads a register during the same clock cycle as another instruction is writing it, the new value will **not** be read. Note that an instruction takes 5 clock cycles to complete (if not stalled). **Do not reorder the instructions.** Instructions are fetched and executed exactly in the order given below.

```
lw    $s1,0($s2)
lw    $t1,0($s1)
addi  $s3,$s1,4
addi  $s1,$t1,-1
add   $t0,$s1,$s1
```



(b) (*4 marks*) Repeat part (a), but now assuming that the pipeline **does** use forwarding, and that if one instruction reads a register during the same clock cycle as another instruction is writing it, the new value **will** be read.

5, 2 + 1 + 1 + 1 = 10

(c) (*4 marks*) Consider the single-cycle, multicycle, and pipelined (with hazard detection, forwarding, and branch prediction) implementations of a MIPS subset discussed in class.

(i) With which of these implementations would you expect to have the highest CPI?

Multicycle

(ii) With which would you expect to have the second highest CPI?

Pipelined

(iii) With which would you expect to be able to achieve the highest clock rate?

Multicycle or pipelined

(iv) With which would you expect to have the lowest clock rate?

Single-cycle

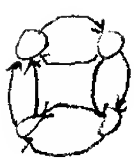
(d) (*4 marks*) In what ways might compiler techniques for dealing with hazards be preferable to hardware approaches? In what ways might hardware approaches be preferable?

Compiler - entire program can be considered and rearranged
- use simpler hardware (increase clock speed)
- simpler to change

Hardware - more powerful
- runtime info on branching
- legacy code (don't have machine code)

(e) (*4 marks*) Describe how dynamic branch prediction can be implemented, and 1-bit and 2-bit dynamic branch prediction schemes.

-branch table (lower address bits), - target address
1 bit : - previous branch decision
2 bit : - remember two previous bits, don't change decision until two "misses"



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6. **Cache and Virtual Memory** (*18 marks in total*)

   (a) (*4 marks*) Consider a cache with space to store 16 blocks.

   (i) Assuming the cache is set associative with each position of the cache having space for 2 blocks, give a formula for the cache position in which memory block number *N* would be stored.

   N mod 8

   (ii) Assuming instead that the cache is direct mapped, and there are 8 words in a block, which cache position would be checked on a reference to (byte) address 1400?

   $\left\lfloor \frac{1400}{8 \cdot 4} \right\rfloor \bmod 16 = 43 \bmod 16 = 11$

   (b) (*4 marks*) State four of the benefits provided by the virtual memory technique.

   - protection
   - sharing (effecient & safe)
   - multiple large programs
   - Single large program
   - flexible memory placement - scatter pages

   (c) (*2 marks*) Suppose that in some system utilizing paged virtual memory, a physical page number is 12 bits, a virtual page number is 48 bits, and a virtual address is 64 bits. What is the maximum amount of physical memory (in Mbytes) that this system could have?

p. 584 Physical Address

Physical Page #	Page offset
$\underbrace{}_{12}$	$\underbrace{}_{64-48=16}$

28 bits 2^{28} bytes   Mbytes

$2^8 \cdot \underbrace{2^8 \cdot 2^8 \cdot 2^4}_{256 \quad 16} = 256 \cdot 256 \cdot 256 \cdot 16 \approx 1\,M$

256 Mbytes

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(d) (*4 marks*) Outline the steps by which a virtual memory address is translated into a physical memory address, in a computer system using the virtual memory technique.

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(e) (*4 marks*) Define temporal and spatial locality, and for each type of locality, give an example of how it is exploited in the management of the memory hierarchy.

Defn. p. 540

temporal LRU

spatial block (eg array